What is claimed is:

- 1. A semiconductor device, comprising:
- a mounting substrate having a step portion in a periphery thereof;
- a conductive pattern formed on a surface of the mounting substrate;
- a semiconductor element fixed to the mounting substrate and electrically connected to the conductive pattern; and

sealing resin covering the surface of the mounting substrate and the step portion to seal the semiconductor element.

- 2. The semiconductor device according to claim 1, wherein the conductive pattern comprises a bonding pad electrically connected to the semiconductor element through a fine metallic wire and a plating line extending from the bonding pad to the step portion.
- 3. The semiconductor device according to claim 2, wherein a plurality of the bonding pads are arranged so as to surround the semiconductor element, further comprising a wiring portion extending from each of the plurality of bonding pads under the semiconductor element.
- 4. A method of manufacturing a semiconductor device, comprising:

forming first conductive patterns which constitute units and common plating lines on a front surface of a substrate, each of the units comprising bonding pads and plating lines extending from the respective bonding pads to a periphery, the common plating lines electrically connecting the plating lines of the units;

forming second conductive patterns on a back surface of the substrate, the second conductive patterns being electrically connected to the respective first conductive patterns;

forming a plated film to a surface of the first conductive patterns by electroplating using the common plating lines;

forming grooves on the front surface of the substrate by dicing the front surface of the substrate including the common plating lines to electrically separate the conductive patterns;

placing semiconductor elements on the front surface of the substrate;

providing sealing resin which fills the grooves and seals the semiconductor elements; and

separating the semiconductor elements by dicing the substrate and the sealing resin at borders of the units.

5. The method of manufacturing a semiconductor device according to claim 4, wherein the units are arranged in a

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matrix, and the common plating lines extend along the borders of the units into a grid.